Remarks

The Office Action dated June 4, 2009 presents the following rejections: claims 1-12 stand rejected under 35 U.S.C. § 102(b) over Flora (U.S. Patent Pub. 5,343,417); and claims 8 and 15 stand rejected under 35 U.S.C. § 112(2) for an informality. Claims 13-14 and 16-19 are noted as being allowed. The Advisory Action mailed on July 20, 2009 indicated that the § 112(2) rejection of claim 8 had been overcome. Applicant traverses each of the remaining rejections per the following discussion, which does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise), and further in view of Applicant's traversals of record as fully incorporated herein.

The § 102(b) rejections over claims 1-12 are improper because the cited Flora '417 reference lacks correspondence to multiple claim limitations and aspects of the claimed invention, including those directed to breaking apart long integers into multiple words and to respectively summing addends from the words. For example, the '417 reference fails to disclose limitations in the independent claims as directed to an adder circuit having a first level for receiving addends of multi-bit words, and that sums addends of different multi-bit words. Applicant has reviewed the '417 reference and cannot ascertain any reference to the term "word" or to the summation of values involving calculations that are based upon such words, at either a general level or as relevant to the claimed invention. In contrast, the '417 reference uses a fixed-length adder to process partial products of a multiplicand and multiplier to produce addends that are passed to lower circuits for a specific calculation. This cited processing approach thus provides no correspondence to aspects of the claimed as directed to processing different words, or to doing so using calculations (outputs) generated from previously-processed words as inputs to later-processed words. The Office Action's attempt to show correspondence to the claimed word-related calculations is further improper, because it is based upon a misconstruction of terms that erroneously equates individual addends with words (*see, e.g.*, page 2 of the Office Action, which erroneously refers to addends such as a_1b_1 as words).

In addition to the above, the Office Action has not attempted to show *prima facie* correspondence to multiple dependent claims, to which Applicant can ascertain no correspondence in the cited or other portions of the '417 reference. For example, the '417 reference does not appear to disclose or contemplate setting a number of adders or to using additional adders at intermediate levels to reduce the overall number of levels, also in the claimed invention. The Advisory Action did not further address Applicant's traversals of the § 102(b) rejection as presented in each of Applicant's prior responses of record. Accordingly, Applicant maintains that there is no basis for the § 102(b) rejections and requests that they be removed.

Lack Of Correspondence As Established In The Record

In view of the above, Applicant again requests that Applicant's previously-presented arguments be considered and addressed as such effort is expected to render all the claims allowable over the art of record. The following summarizes the impropriety of these rejections as consistent with Applicant's responses of record.

The '417 reference makes no mention whatsoever of circuits, as claimed by Applicant, for summing addends from multi-bit words and/or any logic circuitry for processing bits from multi-bit words, as relevant (for example) to summing a succession of words in long integers for multiplying the integers. Referring to column 5:12-27, the '417 reference also defines its adder 21 as having a bit-length that is unrelated to multi-bit words, as consistent with long-standing ordinary/dictionary definitions that differentiate commonly-used technical terms such as "bits", "bytes" and "words" (*see, e.g.*, paragraphs 003-004 of Applicant's specification and the cited '417 reference at column 2:40-51). This adder bit-length as well as the number of adders must be fixed in the '417 reference, to suit its purpose relating to setting the number of stages in respective adders and using a built-in delay to permit the use of a half-adder to save space (*see* columns 1:19-22 and 5:31-36). Moreover, the '417 reference goes on to explain that the particularly taught implementation involves a full-adder versus half-adder approach with deficiencies towards its purpose due to the manner in which the full adder is used. See '417 reference at column 4, lines 51 *et seq.* In an effort to address these deficiencies and achieve the above-noted purpose, the '417 reference teaches that a final level (level 4)

includes a pair of adders (serial adder 20 and carry look-ahead adder 21) arranged such that the specific length of serial adder 20 permits for faster processing by carry look-ahead adder 21 and less circuit-board real estate to implement adder 21. See '417 reference at column 5:37-51, column 1:37-41. Accordingly, the rejection should be removed because the '417 reference is directed to a specific type of implementation that neither corresponds to the claimed invention nor applies to the type of environment (summing multi-bit words) set forth as part of the claimed invention.

Applicant further submits that the teachings of the '417 reference are so specific in this regard, the skilled artisan would be led away from any suggestion of attempting to use such teachings in a manner as asserted in the Office Action. See the cited '417 reference generally, including relevant discussion at column 5:18-22, as well as M.P.E.P. § 2143.01.

Lack Of Correspondence To The Amended Claims

Applicant submits that the § 102(b) rejections are further improper in view of the amendments presented herein, as also consistent with the above discussion. For example, amended claim 1 includes limitations directed to at least one of the levels receiving addends corresponding to a calculation involving another one of the words (in connection with the summing of words). Support for this amendment may be found in claim 1 as filed ("summing a plurality of addends from multi-bit words"), and throughout the specification and figures, with exemplary embodiments described in paragraph 0100. New claims 21-25 depend from claim 1 and are believed to be allowable over the cited references for reasons including those stated above, and further because the '417 reference fails to disclose limitations directed to splitting integers into multi-bit words, and processing the words and using addends from calculations involving one of the words in the processing of another one of the words.

The § 112(2) Rejection Is Improper

Applicant believes that the remaining § 112(2) rejection of claim 15 is improper because it appears to be based upon a misinterpretation of the claim and the use of the term "by" in characterizing a calculation. Specifically, the claim recites that a carry bit is

used after a subsequent calculation of "first and second low order parts by the first summation means." As such, the first and second low order parts are calculated by the first summation means. In contrast, the rejection appears to be based upon a reading of the claim as reciting that the carry bit is used "by the first summation means" without addressing the limitations "first and second low order parts" as recited above. Accordingly, Applicant believes that claim 15 is clear in view of the above. Applicant has also amended claim 15 in an effort to assist the Examiner's understanding and facilitate prosecution, yet believes that the scope of the amended claim 15 is consistent with the claim, prior to amendment (and that such amendment is unnecessary for patentability). Applicant believes that the § 112(2) rejection is no longer applicable and requests that it be removed.

In view of the above, Applicant believes that each of the rejections has been overcome and/or is inapplicable, and further that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney overseeing the application file, Juergen Krause-Polstorff of NXP Corporation at (408) 474-9084 (or the undersigned).

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